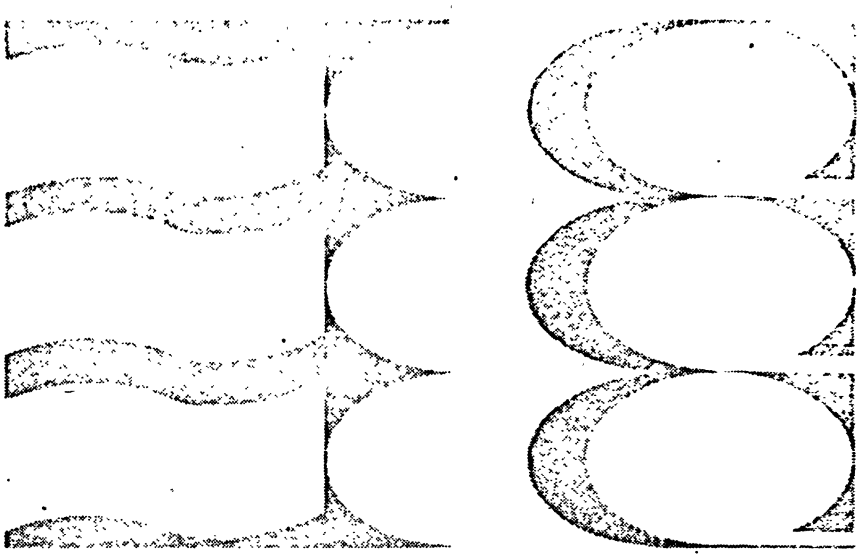

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92/9300 SLAVE CHANNEL ADAPTER (F1001-01)
PROGRAM DESCRIPTION DRAWING

4091650

DRAWING NUMBER 4091650

REVISION A

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9300 SLAVE CHANNEL ADAPTER (F1001-01)
PROGRAM DESCRIPTION DRAWING

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APPROVAL			

Associated listing is Revision A

REVISION STATISTICS RECORD 4091650

DWG REV	MSTR REV	RELEASE DATE	DESIGNER NAME	EIR NUMBER	FCO NUMBER
-	F	10/10/69	W. R. Karban	A89798	A30190029
A	G	3/[illegible]/71	W. R. Karban	A89800	A301900300
B	P	2/7/74	G. Chin		

REVISION RECORD 4091659

REV	DESCRIPTION
-	Release
A	Correct typing errors, table of contents etc. Corrections to tests 19 and 20 after hardware was debugged. Add changes to operate with 92/9300 Master Program (Document #4091656).
B	An option was incorporated for the selection of a 96 character print bar.

4091650

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1.0 INTRODUCTION

1.1 Purpose - This document describes the 9300 Slave test which checks the Channel Adapter 9000 (F1001-01).

1.2 Major Objectives - This MAR is designed to perform a functional test of the 9000 Series Channel Adapter.

1.3 Equipment Configuration - This MAR is used with the following equipment configuration:

9400 Processor with Multiplexer (MPX) I/O Channel

9000 Series Channel Adapter

9200/9300 Processor with General Purpose I/O Channel

1.4 Associated Software - This program relies on the standard four card Engineering Loader to perform program load. It is used with the 9400 Master Channel Adapter Test Master Program (Drawing Number 4091649) or the 9300 Master Channel Adapter Test Program (Drawing Number 4091656) to complete the interface checkout of the Channel Adapter 9000.

1.5 Reference Documents - Documents used as reference material for the development of this test program are listed below.

Drawing	Revision	Description
SU00039		9000 Series I/O Interface Equipment Specification
S-90065		F1001-01 Channel Adapter Product Description
S-70040		9400 Processor and Console Product Description
4091622		9400 Maintenance Control Routine Program Description Drawing
4091649		9400 Channel Adapter Test Program Description
P-1ØØ44	D	9200 System Type 3030-00, -01
		TECH MEMO 699-01
		TECH MEMO 699-02
4091656		9300 Master Channel Adapter Test Program

1.6 Program Notes and Restrictions -

1.6.1 "Time Out" Information - This program provides no "Time Out" information for the operator, i.e., there is no message to indicate an operation has taken more than a specific amount of time. Therefore, the operator should take note of the following information:

When operating with the 9400 Master adapter program, the 9400 Master, through the MCR, provides "time out" information.

When operating with the 9300 Master, the display register indicators will appear to change in intensity (flash) if the program is running normally. A "time" abnormality will generally be preceded by some other error message and/or the display register lights will appear to remain at one address, with several of the lights extinguished. This is caused by the program waiting for an I/O transfer to be completed.

1.6.2 Other Notes - This program exits from a test if an error occurs. The "Master" and "Slave" are mutually dependent for information, except for "off-line" testing. Because an error in one test or the other may cause an error in the other program, the operator should note all error messages very carefully. An example of this is the "Slave" side of the adapter not receiving an "Attention" even though there was no error from the Master program.

The Adapter may become "hung" due to malfunction. Due to adapter design, the adapter cannot be cleared by the processor in "Control" mode. The only recourse in this case is to clear both the processor and the adapter, and restart the programs.

If an error occurs in this program, this program exits from the test being executed and either waits for an interrupt, if interfacing the 9400 Master, or returns to the master in the 92/9300. The "Off Line" test excluded, of course.

2.0 FUNCTIONAL DESCRIPTION

2.1 General - This MAR interfaces a "Master" program which controls which tests are executed. Selection of the subchannel(s) which have (an) adapter(s) to be tested is described in paragraph 3.3.

Initially the adapter checks the following commands in Idle Mode:

Test I/O command
Test I/O Override command
Sense command
Illegal command
No-Op command.

These tests are referred to as "Off-Line" tests since they are independent of the "Master" program. This is opposed to the Idle Mode tests 15 through 20.

The commands are tested on the subchannel(s) whose "run" flag has been set by the operator. Once this initial testing is completed, this program executes tests depending on test selection in the Master program. Test selection is matched as follows:

Master Program Test #	Slave Program Test #
5	2
6	2
7	3
8	4
10	5
11	6
12	7
13	8
14	9
15	10
16	11
17	12
18	13
20	14
21	16
22	17
23	18
24	19
25	15
26	2Ø

The Master program sends a command, with detail bits set, to the Slave program. This command should result in an "Attention" interrupt to the Slave program. The Slave program responds to the Attention with a Sense command. The sense byte should contain the command and detail bits sent from the Master program. The sense byte is checked for one of several values of command and detail bits. If no comparison can be found, the Slave program cannot execute any test on the adapter.

Because Adapter design does not allow the Test I/O Override command to terminate the adapter from the same processor in "Control" of the adapter, the adapter may become "hung" and must be manually cleared. The programs, on order to maintain some order, cannot arbitrarily issue a Test I/O Override in case of an error.

2.2 Test Descriptions - Each of the following tests is described by stating its objective and the method used to attain it.

2.2.1 Test 1 (Undefined) - Test 1 remains undefined at this time.

2.2.2 Test 2 - Minimum Write Command Test - ("Master test 5 and 6)

Objective:

Test adapter acceptance of a Write command in response to a Read command from the Master program.

Method:

1. A Write command with a buffer length of 1 byte is sent to the adapter.
2. The condition code after the XIOF is expected to be zero.
2. The status is expected to be Channel End - Device End.

2.2.3 Test 3 - Minimum Read Command Test - ("Master" test 7)

Objective:

Test adapter acceptance of a Read command in response to a Write command from the Master program

Method:

1. A Read command with a buffer length of 1 byte is sent to the adapter.
2. The condition code after the XIOF is expected to be zero.
3. The status is expected to be Channel End - Device End.
4. If the status is correct, the input data is checked for a value of Ø3.
5. If the input byte is not Ø3 the processor will halt.
6. Depress "start" to continue testing.

2.2.4 Test 4 - Test Transfer of Control Command from the Master Program - ("Master" test 8)

Objective:

Test that the Control command may be transferred from the Master program with all combinations of detail bits.

Method:

After executing a Sense command in response to a Control command from the Master program, the Control command is checked for the correct value as follows:

1. An index is used to form the detail bits. This index is "or'ed" with the Control command and is checked against the value of the sense byte received.

2. For each subsequent value of detail bits, the index is decremented by 1 as in the Master program.

NOTE: The Slave program determines that the Control command is being tested by checking bits 6 and 7 of the Sense byte both equal to "1", i.e., the sense byte = $xxxxxx11_{16}$.

2.2.5 Test 5 - Write Test #1 - ("Master" test 1Ø)

Objective:

Test data transfer from the Slave program to the Master program with a data pattern of alternate bytes of "ones" and zeros.

Method:

This test proceeds as test 2, paragraph 2.2.2, except as follows:

1. The data pattern = FF00. . .
2. The buffer length is 16Ø bytes.

2.2.6 Test 6 - Write Test #2 - ("Master" test 11)

Objective:

Test data transfer from the Slave program to the Master program with a "bit-no bit" data pattern.

Method:

This test proceeds as test 2, paragraph 2.2.2, except as follows:

1. The data pattern = AAA . . .
2. The buffer length is 16Ø bytes.

2.2.7 Test 7 - Write Test #3 -("Master" test 12)

Objective:

Test transfer of all 256 bit combinations from the Slave program to the Master program.

Method:

This test proceeds as test 2, paragraph 2.2.2, except as follows:

1. The data pattern is 255 compress mode characters.
2. The four data buffers of 80 bytes each are used. The 4th buffer is padded with zeros.

NOTE: Each data buffer requires a Read command from the Master program.

2.2.8 Test 8 - Test Adapter with Operator Specified Data - ("Master"test 13)

Objective:

Allow the operator to select 2 bytes of data as the data pattern.

Method:

This test proceeds as test 2, paragraph 2.2, except as follows:

1. Two bytes of data specified by the operator are used for the data pattern. The 2 bytes are repeated throughout the buffer, i.e., if the operator data - 3F4E the data buffer would be 3F4E3F4E3F4E . . .
   The 2 bytes of specified data are entered into address 5F4 and 5F5.
2. The buffer length is 16Ø bytes

2.2.9 Test 9 - Write Test #4 - ("Master" test 14)

Objective:

Test transfer of all "ones" (FFF . . .) from the Slave program to the Master program.

Method:

This test proceeds as test 2, paragraph 2.2.2, except as follows:

1. The data pattern is all "ones".
2. The buffer length is 16Ø bytes.

2.2.10 Test 10 - Write Test #5 - ("Master" test 15)

Objective:

Test data transfer of all zeros from the Slave to the Master program.

Method:

This test proceeds as test 2, paragraph 2.2.2, except as follows:

1. The data pattern is all zeros.
2. The buffer length is 16Ø bytes.

2.2.11 Test 11 - Test Terminate of Read Command -("Master" test 16)

Objective:

Test use of Test I/O Override command to terminate the adapter after a Read command is sent by the Master program.

Method:

1. A test I/O Override command is issued.
2. The condition code after the XIOF is checked for zero.

2.2.12 Test 12 - Test for Busy and Attention Status - ("Master" test 17)

Objective:

Test that the adapter responds with a "Busy and Attention" status if a Read Backward command is received from the Master program and is answered with a Read Backward command from the Slave program.

NOTE: This test could be made by responding to a Write command with a Write Command. The choice of the Read Backward command was arbitrary.

Method:

1. The Read Backward command is sent to the adapter.
2. The condition code is checked after inspecting the XIOF for one.
3. The status is checked for "Busy and Attention" ($9\emptyset_{16}$).
4. A Test I/O Override command is sent to clear the adapter.
5. The condition code is checked, after issuing the XIOF, for zero.

2.2.13 Test 13 - Test Terminate of a Write Command - ("Master" test 18)

This test is the same as test 11, paragraph 2.2.11, except the Master program sends a Write command.

2.2.14 Test 14 - Test Terminate of Data mode - ("Master" test 19)

Objective:

Test terminate of Data mode by issuing a Test I/O Override command to the adapter while the adapter is in the Data mode.

Method: Master program in 9400

1. A write command is sent to the adapter.
2. The condition code after executing the XIOF is checked for zero.
3. The status is checked for Channel End - Device End - Unit Check ($\emptyset C_{16}$)
4. A sense command is sent to the adapter.
5. After executing the XIOF the condition code is checked for zero.
6. Status is expected to be Channel End - Device End ($\emptyset C_{16}$).
7. The sense byte is checked for the Reject bit set ($\emptyset 2$).

Method: Master program in 92/9300

After step 2 return to the Master program. The Master program then returns to Slave and Slave continues from step 3.

2.2.15 Test 15 - Slave Program Idle Mode Test #1 - ("Master" test 25)

Objective:

Test the Test I/O and Test I/O Override commands in Idle mode from the Slave program.

Method: Master program in the 9400

1. A Test I/O Override command is used to terminate the adapter.
2. The condition code, after executing the XIOF, is checked for zero.
3. A Test I/O Command is sent to the adapter.
4. The condition code, after executing the XIOF, is expected to be zero.
5. A Test I/O Override command is sent to the adapter.
6. After the XIOF, the condition code is checked for zero.

Method: Master program in 92/9300

After step 2, return to the Master program. The Master program then returns to Slave and Slave continues from step 3.

2.2.16 Test 16 - Slave Program Idle Mode Test #2 - ("Master" test 21)

Objective:

Test the No-Op command for the Slave program.

Method: Master program in the 9400

1. A Test I/O Override command is sent to terminate the adapter.
2. The condition code, after executing the XIOF, is checked for zero.
3. A No-Op command is sent to the adapter.
4. The condition code is checked after issuing the XIOF, for zero.
5. The status is checked for Channel End - Device End.

Method: Master program in 92/9300

Same as for test 15, paragraph 2.2.15.

2.2.17 Test 17 - Slave Program in Idle Mode Test #3 - ("Master"test 22)

Objective:

Test Sense command in Idle Mode, from the Slave program.

Method: Master program in the 9400

1. A Test I/O Override command is sent to the adapter.
2. The condition code is checked for zero after the XIOF.
3. A sense command is sent to the adapter.
4. The condition code, after the XIOF, is checked for zero.
5. The status is checked for Channel End - Device End.
6. The sense byte is checked for a value of zero (Ø).

Method: Master program in 92/9300

Same as for Test 15, paragraph 2.2.15.

2.2.18 Test 18 - Slave Program Idle Mode Test #4 - ("Master" test 23)

Objective:

Test the Illegal command ($\emptyset 8_{16}$) in Idle mode from the Slave program.

Method: Master program in the 9400

1. A Test I/O Override is sent to the adapter.
2. After the XIOF the condition code is checked for zero.
3. The Illegal command is sent to the adapter.
4. After the XIOF, the condition code is checked for zero.
5. The status is checked for Unit Check ($\emptyset 2$).
6. A Sense command is sent to the adapter.
7. The condition code is checked, after the XIOF, for zero.
8. The status is checked for Channel End - Device End.
9. The sense byte is checked for Command Reject bit set ($8\emptyset_{16}$).

Method: Master program in the 92/9300

Same as for Test 15, paragraph 2.2.15.

2.2.19 Test 19 - Slave Program Control Command Test - ("Master test 24)

Objective:

Test the control command by issuing the Control Command from the Slave program.

Method: Master program in the 9400

1. A Test I/O Override is sent to the adapter.
2. The condition code, after the XIOF, is checked for zero.
3. A Control Command ($\emptyset 7_{16}$) is sent to the adapter.
4. The condition code, after the XIOF, is checked for zero.
5. The status is checked for Channel End ($\emptyset 8_{16}$).
6. The program waits for Device End status which should be caused by the Master program executing a Sense command. The Master program sends the Sense command approximately one second after sending the command to the Slave program to start the Control Command test.

Method: Master program in the 92/9300

After step 2, Slave returns to the Master. Master returns to the Slave and Slave executes steps 3, 4, and 5. Slave returns to Master. Master returns to Slave and Slave does step 6. The one second delay is omitted.

2.2.20 Test 2Ø - Slave Program "Immediate Busy" Test - ("Master" test 26)

Objective:

Test that the adapter returns an "Immediate Busy" status if a command is sent to the adapter before the previous command has received end status.

Method: Master program in the 9400

1. A Test I/O Override command is sent to the adapter.
2. After the XIOF, the condition code is checked for zero.
3. A Write command is sent to the adapter.
4. The condition code is checked, after the XIOF, for zero.
5. A Read command is sent to the adapter.
6. The condition code, after the XIOF, is checked for busy (Ø2).
7. The status is checked for Immediate Busy ($5Ø_{16}$).
8. End status is checked for Channel End - Device End - Unit Check ($ØE_{16}$). This status is caused by the Master program sending a Test I/O Override to the adapter. The Test I/O Override is sent approximately one second after the Master program starts the Immediate Busy test.

Method: Master program in 92/9300

After step 2, Slave returns to the Master. Master returns to Slave and Slave executes steps 3, 4, 5, 6, and 7. Slave returns to Master. Master returns to Slave and Slave completes Step 8. The one second delay is omitted.

2.2.21 Slave "Off-Line" Tests -

Objective:

Allow testing of the adapter in Idle Mode "Off-Line".

Method:

The test procedure is the same as for tests in paragraphs 2.2.15, 2.2.16, 2.2.17 and 2.2.18 except the Test I/O Override, Steps 1 and 2 in the method description is not sent as the adapter is in Idle mode. Tests are as follows:

Test #F1 = Test "Test I/O" Command
Test #F2 = Test "Test I/O Override" Command
Test #F3 = Test "No-Op" Command
Test #F4 = Test "Sense" Command
Test #F5 = Test "Illegal" Command

NOTE: These tests are available on load, but may be deleted. See paragraph 3.3.

[illegible] -

[illegible] loading the program, the operator should ascertain the configuration the Channel Adapter is cabled for. Cabling may be as follows:

1. If using the 92/9300 Master program, the adapter must be cabled "Back to Back" on different 92/9300 Channels, e.g., the Master program on Channels B, the Slave program on Channel C.

2. If using the 9400 Master program, the 9400 must have 1 MUX subchannel cabled to a 92/9300 channel.

After checking the cable configuration, the operator should check that power has been applied to those equipments to be used.

3.2 Program Loading - To load the Slave object deck, proceed as follows:

1. Place the 4 card loader followed by 1 blank card in front of the object deck.
2. The object deck should be followed by 1 blank.
3. Set data entry switch(es) to select the card reader.
4. Depress both processor clear and channel clear.
5. Clear reader and feed one card.
6. Set "load" switch and depress "start".
7. Clear "load" switch and depress "start".
8. Object deck should read in and the computer stop with the Halt - Display register = DE_{16}.
9. Depress reader "feed".

3.3 Program Parameters - Parameters are entered by altering storage within the 92/9300 Slave Adapter test locations (in hexadecimal). Their setting and interpretation is as follows:

Address	Value	Interpretation
Ø250	ØØ	Master test is in 9400.
Ø250	Ø1	Master test is in 92/9300. (Set by the 9300 Master Test)
Ø251	ØØ	Cycle "Off-Line" mode tests once on each 92/9300 subchannel that has its "Run" flag set. Subchannel selection is from lowest to highest.
Ø251	Ø1	Cycle "Off-Line" mode tests continuously for those subchannels that have their "Run" flag set. Subchannel selection is from lowest to highest and back to lowest.

Address	Data	Interpretation
Ø25Ø	ØØ	Print error messages.
Ø252	Ø1	Do not print error messages.
Ø253	ØØ (Preset)	Print Bar - 64 Characters
Ø253	Ø1	Print Bar - 96 Characters

Addresses Ø254 through Ø258 contain flags for the "Off-Line" tests. The flags are preset on load, to be executed.

Ø254	F1	Run test F1.
Ø254	ØØ	Do not run Test F1.
Ø255	F2	Run test F2.
Ø255	ØØ	Do not run test F2.
Ø256	F3	Run test F3.
Ø256	ØØ	Do not run test F3.
Ø257	F4	Run test F4.
Ø257	ØØ	Do not run test F4.
Ø258	F5	Run test F5.
Ø258	ØØ	Do not run test F5.

Ø259 through Ø263 are subchannel "Run" flags. To use the Adapter on a subchannel, set the subchannel "Run" flag to Ø1, otherwise set it to ØØ. The program is preset on load with all "Run" flags = ØØ.

Address	Subchannel
Ø259	5
Ø25A	6
Ø25B	7
Ø25C	8
Ø25D	9
Ø25E	A
Ø25F	B

Address	Subchannel
Ø26Ø	C
Ø261	D
Ø262	E
Ø263	F

Ø264 is a flag for "Off-Line" tests in case of an error message. This flag is set to FF ON LOAD and is cleared after executing all off-line tests and address Ø251 is zero.

Ø264 = FF	Off-Line tests not completed. Return to Off-Line tests after an error.
Ø264 = ØØ	Off-Line tests not active.
Ø266 Ø267	2 bytes entered by the operator are used as data for test 8. The same pattern must be used for the Master program test 13.

Address	Value	Interpretation
A88	$A9_{16}$	Halt processor after error messages - available on load.
A88	47_{16}	Do not halt processor after error message.

3.4 Parameter Notes and Restrictions - Parameters should be changed with the 92/9300 processor in the "Stopped" state. This will avoid having any flags in the improper state. After changing parameters the program should be restarted per paragraph 3.7.

3.5 Program Starting - After using the load procedure in paragraph 3.2, proceed as follows:

1. Select program parameters per paragraph 3.3
2. Depress both "clear" and "channel clear".
3. Clear channel adapter.
4. Depress start unless the "Off-Line" test parameters have been changed. The program executes the following tests once with the adapter in the Idle mode, then waits for an interrupt from the Master program.

   #F1 = Test I/O command
   #F2 = Test I/O Override command
   #F3 = No-Op command
   #F4 = Sense command
   #F5 = Illegal command

If the Master program is to be in the 92/9300 the Master program may be loaded at this time, using the same load procedure as paragraph 3.2. Parameters for the Master may be obtained from the Master program description (Drawing number 4091656).

When the master program is started it branches to the Slave program. The Slave program executes tests F1, F2, F3, F4 and F5 per parameter settings. The Master program sets the Slave "Off-Line" flag prior to branching to the Slave. When the Slave completes the "Off-Line" testing it returns to the Master program.

3.6 Program Stopping - The program may be stopped as follows:

1. If the "Master" program is in the 92/9300 processor, depress "stop" on the 92/9300.

2. If the "Master" program is in the 9400 processor, stop the 9400 test first, then stop the 92/9300 processor.

3.7 Program Restarting - The program may be restarted as follows:

1. If the "Master" program is in the 92/9300 depress "computer" clear and "channel" clear, depress "start".

2. If the "Master" program is in the 9400 processor, start the 92/9300 test per step 1 above, then start the 9400 program.

3.8 Mnemonics - The mnemonics used in the error messages are defined below.

A92/9300S	= Program Name
PC	= Previous Command
CC	= Current Command
PS	= Previous Status
CS	= Current Status
ES	= Expected Status
PSB	= Previous Sense Byte
ESB	= Expected Sense Byte
CSB	= Current Sense Byte
Sn	= Subchannel (Device) n (Hexadecimal)
Tn	= Test n (Decimal)
EXP	= Expected
ACT	= Actual

3.9 Error Messages - Error messages are printed on one line. The following messages may occur: ATTENTION ERROR. Status = nn, Device = nn.

This message is printed if the interrupt received while waiting for a command from the Master program does not result in "attention" status ($8\emptyset_{16}$).

DEVICE REQUESTED is Inactive. DEVICE = nn

This message occurs if an "Attention" interrupt is received on a subchannel that does not have its "Run" flag set.

Tn Sn CONDITION code error on XIOF PC = nn CC = nn
Exp. Code = n Act Code = n

The condition code that is set as a result of a command sent to the adapter is checked for an expected value. An unexpected condition code is an error and results in this message.

Tn Sn Status Error PS = nn CS = nn ES = nn PC = nn CC = nn

This message occurs if the status resulting from a command sent to the adapter is not as expected.

Tn Sn Sense Byte Error PSB = nn CSB = nn ESB = nn PC = nn CC = nn

This message is the result of one of two conditions as follows:

1. If the Test Number is $\emptyset$ or 7, and the Expected Sense Byte is zero, the sense command was executed in response to an attention interrupt. The sense byte did not contain any of the expected values to select a test.

2. Some tests require a sense command to determine correct operation of the adapter. In this case, the test number will be other than $\emptyset$, but may be 7. The value of the Expected Sense Byte is other than zero.

4.0 SUPPLEMENTARY DATA

4.1 Supplementary Hardware Information - The Channel Adapter 9000 (CA 9000) is an asynchronous logic device that provides a half-duplex connection between two processor channels. It is capable of controlling data transfer over either a Multiplexer or a Selector Channel, but is restricted to Multiplexer operation by the 9400 Processor.

4.2 Supplementary Software Information - This portion of Section four deals with the operation of the Channel Adapter from a software point of view. In the following subparagraphs, it describes 1) the three modes of operation and 2) the operation of the Adapter under error conditions.

4.2.1 Idle Mode - The Channel Adapter is in the Idle Mode when it has not recognized an Initial Selection Sequence from either channel or when it does not have Pending Status. Detailed information on the status reply to commands issued by either channel when in the Idle mode is shown in Table 1 of the F1001-01 Channel Adapter 9000 Product Description.

4.2.2 Control Mode - The Channel Adapter is in the Control mode when it is busy but has not yet detected a "match" between the two processors. A match occurs, for example, if Processor A issues a Write Command and Processor B, after sensing, issues a Read Command.

4.2.3 Data Mode - The Channel Adapter is considered to be in the Data Mode upon recognition of a match. When in this mode and transferring data, the Adapter appears busy to both processors until the transfer operation is terminated. It responds with a Busy Status to all commands except the Test I/O Override command.

Termination of the operation in progress can be accomplished by Command Out response to a Service In signal, a Selective Reset condition, a Test I/O Override command, or an Interface Disconnect Sequence. When a Command Out response to a Service In signal (from either processor) is detected in the Adapter, it sends a status byte containing Channel End and Device End information to both processors.

When a Selective Reset condition occurs, Channel End, Device End, and Unit Check will be sent to the processor not causing the Selective Reset. A sense byte containing Equipment Check information will also be sent to that processor.

If a Test I/O Override command is sent to the Channel Adapter when it is operating in the Data mode, it replies with a status byte containing Channel End and Device End. It then sends a status byte and a sense byte to the opposite processor. The status byte has Channel End, Device End, and Unit Check set; the sense byte has the Reject bit set.

If the Channel Adapter detects an Interface Disconnect Sequence while operating in the Data mode, it sends Channel End and Device End status to both processors. A Unit Check will also be sent if an error condition occurred.

4.2.4 Error Conditions - This paragraph describes the operation of the Channel Adapter under three error conditions. Each error condition is defined and the related operation described in the space below.

Command Parity Errors - This type of error occurs on commands during the Initial Selection Sequence. The Adapter sends a Unit Check and a Bus Out Check to the processor in error. The opposite processor is sent both a Channel End, Device, End and Unit Check Status and a sense byte containing Equipment Check.

If the Adapter is not in the Data Mode when the error occurs, it will send the same sense information to the opposite processor but the status byte will contain only Unit Check and Attention Status. A Bus Out Check causes immediate termination in all cases.

Data Parity Errors - This type of error occurs during data transfer. Upon detection of a parity error, the Adapter sends status and sense bytes to both processors. The status byte contains Unit Check, Channel End, and Device End. The sense byte has the Data Check bit set. The originating processor will resend the last byte as soon as it receives the Data Check.

Illegal Command - If an illegal command is detected by the Adapter, a Unit Check followed by a Command Reject is sent to the processor in error.

4.2.5 Normal Command Sequence for Data Transfer -

Read Command From Processor A	Initial Selection Sequence
"0" Status to Processor A	
Attention Status to Processor B	Request in Status
Sense Command from Processor B	Initial Selection Sequence
"0" Status to Processor B	
Sense Byte to B (Sense Byte contains Read Command From A)	Request in Data
Status to Processor B (Channel End, Device End	Request in Status
Write Command from Processor B	Initial Selection Sequence
"0" Status to Processor B	
Data Request to Processor B (Output Byte from B)	Request in Data
Data Request to Processor A (Input Byte from A)	Request in Data
Data Request to Processor B (Output Byte from B)	Request in Data
Data Request to Processor A (Input Byte to A)	Request in Data
*Data Request to Processor B (Command out Response to Service In (terminate))	Request in Data
Status to Processor A & B (Channel End, Device End)	Request in Status

* Terminate could occur from Processor A or B

4.2.6 Normal Sequence for Control Command Transfers -

Control Command from Processor A	Initial Selection Sequence
Status to Processor A (Channel End)	
Attention Status to Processor B	Request in Status
Sense Command from Processor B	Initial Selection Sequence
"0" Status to Processor B	
Sense Byte to B (Sense Byte contains Control Command from A)	Request in Data
Status to Processor B (Channel End, Device End)	Request in Status
Status to Processor A (Device End)	Request in Status

4.2.7 This paragraph consists of three tables which define and illustrate the different Command, Status, and Sense Bytes.

Where: P = Odd parity bit

D = Command detail bit

TABLE 1. Command Repertoire

COMMAND	P 0 1 2 3 4 5 6 7	PURPOSE OF COMMAND
READ	P D D D D D D 1 0	Conditions the adapter to generate Attention Status to the opposite channel. A sense then a write command could be the appropriate response to Attention.
READ BACKWARD	P D D D D 1 1 0 0	Conditions the adapter to generate Attention Status to the opposite channel. A sense then a write command would be the appropriate response to Attention.
WRITE	P D D D D D D 0 1	Condition the adapter to generate Attention Status to the opposite channel. A sense then a read command would be the appropriate response to Attention.
CONTROL	P D D D D D D 1 1	Conditions the adapter to generate Attention Status to the opposite channel. A sense command would be the appropriate response to Attention. At least one of the detail bits must be set.
SENSE	P D D D D 0 1 0 0	Conditions the adapter to input one sense byte to the channel that issued the command.
TEST I/O	P 0 0 0 0 0 0 0 0	Command used to obtain the present status of the channel adapter. Command does not cause generation of new status.
TEST I/O OVERRIDE	P 0 1 0 0 0 0 0 0	Command used to clear existing conditions in the adapter. (Multiplexer Channel only).
NO-OP	P 0 0 0 0 0 0 1 1	Used in test programs to exercise the minimum amount of control unit hardware.

TABLE 2. Status Byte Repoertoire

STATUS BYTES	P 0 1 2 3 4 5 6 7	PURPOSE OF STATUS BYTE
ATTENTION	P 1 0 0 0 0 0 0 0	To inform the processor that a command is being held in the adapter register. (Sense command must be issued to obtain command byte.)
BUSY	P 0 0 0 1 0 0 0 0	Indicates that a previously initiated command is still in progress or that the adapter was holding pending status.
CHANNEL END	P 0 0 0 0 1 0 0 0	Indicates that part of an operation is complete.
DEVICE END	P 0 0 0 0 0 1 0 0	Indicates completion of an operation.
UNIT CHECK	P 0 0 0 0 0 0 1 0	Indicates an error condition has been detected by the adapter. The sense byte is conditioned to indicate this error.

TABLE 3. SENSE BYTE REPERTOIRE

SENSE BYTES	P 0 1 2 3 4 5 6 7	PURPOSE OF SENSE BYTE
COMMAND REJECT	P 1 0 0 0 0 0 0 0	Indicates that an Invalid Command was detected by the Channel Adapter.
BUS OUT CHECK	P 0 0 1 0 0 0 0 0	A parity error exists on a command.
EQUIPMENT CHECK	P 0 0 0 1 0 0 0 0	Indicates that a Selective Reset or Bus Out Check occurred on the opposite processor.
DATA CHECK	P 0 0 0 0 1 0 0 0	Indicates that a Channel Parity Error existed in the last data transfer. Data check will be presented to both processors.
REJECT	P 0 0 0 0 0 0 1 0	Indicates that a Test I/O Override was generated by the opposite processor or an Interface Disconnect occurred on the opposite processor before a "Match".